Acsip

AI5018H

Data Sheet

Document History

Date	Revised Contents	Revised by	Version
2023-Dec.-08	Initial release	Max	V1.0A

Content

1 DESCRIPTION

AI5018H is an IPQ 5018 SoC based Wi-Fi 6 System-on-Module (SoM). It is a compact, integrated module that combines all the components required for building a complete system into a single form factor. AI5018H is designed to simplify the process of designing and manufacturing embedded devices and wireless communication systems. With its high-performance processor, memory, storage, and networking capabilities, the AI5018H SoM is well-suited for a wide range of applications, including IoT, networking, and wireless communications. By incorporating all the necessary components into a single module, the AI5018H SoM reduces the time-to-market and overall cost of the end product, making it an attractive solution for many different types of embedded systems.
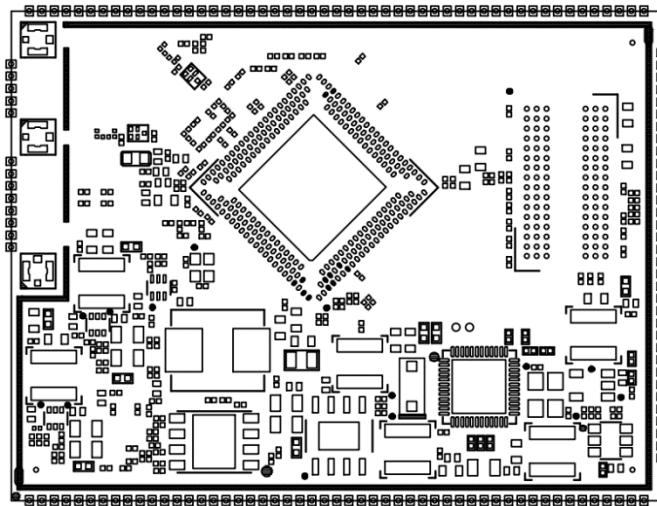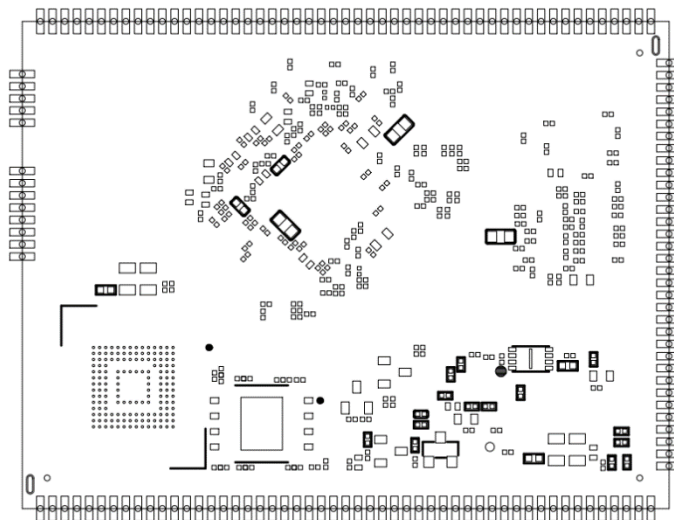
Figure 1 Top Side (Top view)

Figure 2 Bottom Side (Top view)

1.1. Platform Features

General

- ARM Cortex A53 MCU with NPU with up to 1.0 GHz clock speed

- 256KB SRAM / 16MB NOR Flash (U-boot)/128MB NAND Flash (for system)

- Crypto engines including AES256 & SHA256 for network security.

- Two UART interfaces with hardware flow control and one UART for debug, all multiplexed with GPIO.

- One SPI slave interface multiplexed with GPIO.

- IEEE 802.11 b/g/n/ax 2x2 MIMO 2.4GHz compliant

- Supports 20MHz,40MHz bandwidth in 2.4GHz

- 802.11ax mode with data rate up to 573.5Mbps

- Greenfield, mixed mode, legacy modes support

- Security support for WEP WPA WPA2 WPA3

- Supports PCIe2.0 two lane for Wi-Fi module.

- Supports USB3.0/USB2.0 for WWAN modules.

- Major internal components please fine Figure 3 for more details.

Feature list			AI5018H
Integrated core	Core type		Dual-core A53@1.0 GHz
	Core clock frequency		1GHz
	Cache		256 KB L2 cache (shared)
Memory	SDRAM		1GB DDR3L
	NOR Flash		16MB
	NAND Flash		128MB
	eMMC (Optional)		8GB
WIFI	IEEE 802.11 b/g/n/ax 2x2 MIMO 2.4GHz		2412-2472MHz
RF Connector	IPEX MHF4 20449-001E-03		3
Peripherals	PWM	Pulse Width Modulation interface	1
	BLSP	UART debug/UART/SPI/I2C	1/1/1/0
	PCIe	2.0 two-lane PCIe interface	1
	USB	USB 2.0	4
	UPHY	2.0 one-lane PCIe interface or USB 3.0	1
	Ethernet	One integrated 1Gbps	1
		One SerDes supporting 3.125/1.25Gbps Ethernet port	1
	Reset	IPQ5018 reset input	1
PCB information	Core board AI5018H		PCB size 53mm x 40mm x 1.2 mm (6 layers)

Figure 3 Major internal components

2 BLOCK DIAGRAM
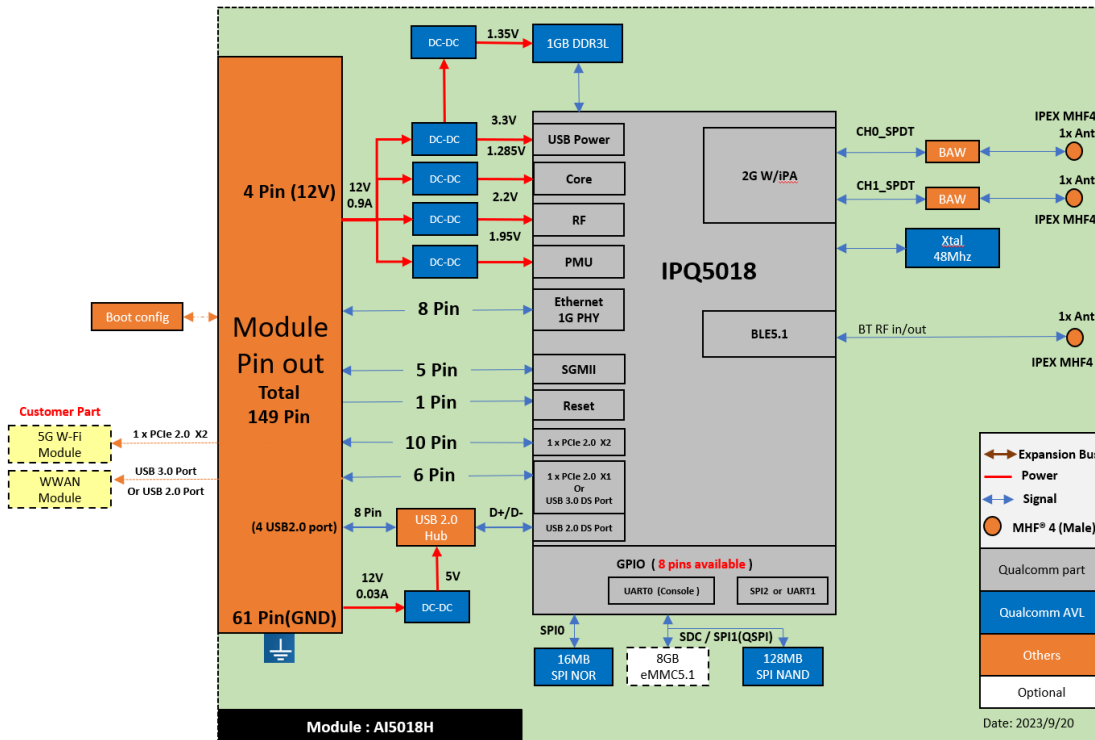
Figure 4 AI5018H block diagram

2.1 SPECIFICATION

AI5018H	
CPU Core	Dual-core ARM Cortex-A53 Clock 1.0 GHz (256 KB L2 cache)
SDRAM	1GB LPDDR3
NAND Flash	128MB
NOR Flash	16MB
Antenna Connector	MHF4 series: 20449-001E-03
Operation Condition	
Junction Operating Temperature (Tj)	0°C ~ + 115°C
Storage Temperature	-40°C ~ + 85°C
Humidity	Operating : 10 ~ 95% (Non-Condensing) Storage : 5 ~ 95% (Non-Condensing)

Mechanical Information	
Dimension	53mm X 40mm X 5.6mm (Typ.)
Package	149Pin - Stamp hole type
Certification	
FCC ID	TBD

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Units
+12V	12 V Input supply voltage	10.8	12	13.2	V

3.2 DC Specification of 1.8V GPIOs

Parameter	Description	Minimum	Typical	Maximum	Units
VIH	High-level input voltage	1.4	-	2.1	V
VIL	Low-level input voltage	-0.3	-	0.45	V
VOH	High-level output voltage	1.6	-	2.0	V
VOL	Low-level output voltage	-0.3	-	0.3	V
IIH	Input high leakage current with no pull-down	-	-	1	uA
IIL	Input low leakage current with no pull-up	-1	-	-	uA
Others	Output-current drive strength	-	-	2	mA

3.3 Power Consumption

Condition			Voltage V	Current A	Total power W
TX	2x2	Throughput at 419Mbps@25°C (Include EK5018H power)	12	0.418	5.016

3.4   RF characteristics

Wi-Fi 2.4G Tx and Rx Specification			
Modulation / Data rate	BW	Tx power (dBm)	Rx Sen. (dBm)
11b / 1Mbps	-	23± 2	-97± 2
11b / 11Mbps	-	23± 2	-88± 2
11g / 6Mbps	20M	23± 2	-93± 2
11g / 54Mbps	20M	18± 2	-75± 2
11n / MCS7	20M	17± 2	-73± 2
11ax / MCS11	20M	15± 2	-64± 2
11n / MCS7	40M	18± 2	-70± 2
11ax / MCS11	40M	15± 2	-60± 2
Bluetooth Specification			
Number of channels	79(BR/EDR)		
	40(LE)		
Modulation	1 Mbps: GFSK (BR)		
	2 Mbps: π/4 DQPSK (EDR)		
	3 Mbps: 8DQPSK (EDR)		
Transmit power	Class 2 BR: 0 dBm ± 2 dB		
	Class 2 EDR: 1 dBm ± 2 dB		
	BLE: 5 dBm ± 2 dB		
Receiver sensitivity (typical values)	BR: -93 dBm ± 2 dB		
	EDR (π/4 DQPSK):-93 dBm ± 2 dB		
	EDR (8DQPSK):-88 dBm ± 2 dB		
	LE: -97 dBm ± 2 dB		

4 Module Pinout and Pin Description

4.1   Detailed Pin Description
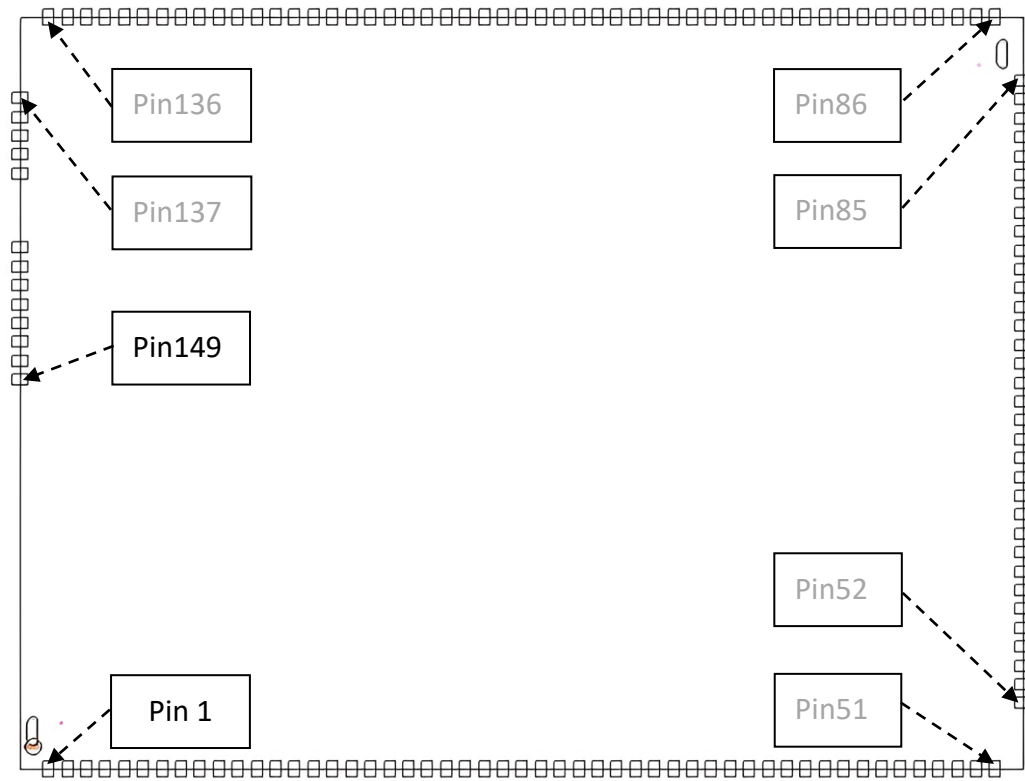
I/O description parameters

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
RF In/Out	RF input/output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal
Z	High impedance

Power and Ground

Pin ID	Pin name	Type	Description
1, 2, 23, 24	12V_IN	I	12V DC Power
4	VDD1V95_PMU	O	1.95V output power for ethernet
3, 5, 10, 15, 22, 25, 28, 31, 36, 41, 44, 47, 52, 55, 58, 61, 64, 65, 73, 74, 75, 76, 77,78, 79, 80, 81, 82, 83, 84, 85, 86, 87,88, 104, 106, 109,112, 115, 118, 121, 124, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 149	GND	GND	Ground
6, 50, 51, 66, 67, 68, 69, 70, 71, 72, 127, 129, 130, 131	NC	NC	Not connected

USB 3.0

Pin ID	Pin name	Type	Description
26	UPHY_REFCLK_OP	NC	NC
27	UPHY_REFCLK_ON	NC	NC
42	CONN_UPHY_RXN	AI	USB3.0_RXN
43	CONN_UPHY_RXP	AI	USB3.0_RXP
45	CONN_UPHY_TXN	AO	USB3.0_TXN
46	CONN_UPHY_TXP	AO	USB3.0_TXP

PCIE2.0 X 2

Pin ID	Pin name	Type	V	Description
29	PCIEX2_REFCLK_OP	AO	1.05	PCIe PHY differential 100MHz reference clock
30	PCIEX2_REFCLK_ON	AO	1.05	PCIe PHY differential 100MHz reference clock
32	PCIEX2_RXN1	AI	1.05	Receiver negative input of the first lane
33	PCIEX2_RXP1	AI	1.05	Receiver positive input of the first lane
34	PCIEX2_RXP2	AI	1.05	Receiver negative input of the first lane
35	PCIEX2_RXN2	AI	1.05	Receiver negative input of the second lane
37	CONN_PCIEX2_TXN1	AO	1.05	Transmitter positive output of the first lane
38	CONN_PCIEX2_TXP1	AO	1.05	Transmitter negative output of the first lane
39	CONN_PCIEX2_TXN2	AO	1.05	Transmitter negative output of the second lane
40	CONN_PCIEX2_TXP2	AO	1.05	Transmitter positive output of the second lane

1GEPHY

Pin ID	Pin name	Type	V	Description
113	MAPLE_TRXN3	IO	1.8	GEPHY signal channel3 signal
114	MAPLE_TRXP3	IO	1.8	GEPHY signal channel3 signal
116	MAPLE_TRXN2	IO	1.8	GEPHY signal channel2 signal
117	MAPLE_TRXP2	IO	1.8	GEPHY signal channel2 signal
119	MAPLE_TRXN1	IO	1.8	GEPHY signal channel1 signal
120	MAPLE_TRXP1	IO	1.8	GEPHY signal channel1 signal
122	MAPLE_TRXN0	IO	1.8	GEPHY signal channel0 signal
123	MAPLE_TRXP0	IO	1.8	GEPHY signal channel0 signal

SGMII

Pin ID	Pin name	Type	V	Description
105	IPQ_SGMII_CLK25M	AO	1.05	Reference clock
107	PHY1_SGMII_TX_N	AO	1.05	Differential output of transmitter. Max data rate = 3.125Gbps
108	PHY1_SGMII_TX_P	AO	1.05	Differential output of transmitter. Max data rate = 3.125Gbps
110	PHY1_SGMII_RX_P	AI	1.05	Differential output of receiver. Max data rate = 3.125Gbps
111	PHY1_SGMII_RX_N	AI	1.05	Differential output of receiver. Max data rate = 3.125Gbps

USB2.0 Port

Pin ID	Pin name	Type	V	Description
53	USB4_HS_DM	B	3.3	USB 2.0 downstream ports 4
54	USB4_HS_DP	B	3.3	USB 2.0 downstream ports 4
56	USB3_HS_DM	B	3.3	USB 2.0 downstream ports 3
57	USB3_HS_DP	B	3.3	USB 2.0 downstream ports 3
59	USB2_HS_DM	B	3.3	USB 2.0 downstream ports 2
60	USB2_HS_DP	B	3.3	USB 2.0 downstream ports 2
62	USB1_HS_DM	B	3.3	USB 2.0 downstream ports 1
63	USB1_HS_DP	B	3.3	USB 2.0 downstream ports 1

GPIO & reset

Pin ID	Pin name	Type	V	Description
7	GPIO_22	IO	1.8	General-purpose digital I/O pin
8	UART_RXD1	IO	1.8	UART debug console
9	UART_TXD1	IO	1.8	UART debug console
11	SPI0_CLK	IO	1.8	Not connected
12	SPI0_MOSI	IO	1.8	Not connected
13	SPI0_CS	IO	1.8	Not connected

Pin ID	Pin name	Type	V	Description

AcSiP Technology Corp.

14	SPI0_MISO	IO	1.8	Not connected
16	EMMC_D3	IO	1.8	Not connected
17	EMMC_D2	IO	1.8	Not connected
18	EMMC_D1	IO	1.8	Not connected
19	EMMC_D0	IO	1.8	Not connected
20	EMMC_CLK	IO	1.8	Not connected
21	EMMC_CMD	IO	1.8	Not connected
48	IPQ_RSTIN_N	I	1.8	IPQ5018 Hardware reset input
49	IPQ_RST_OUT_N	IO	1.8	General-purpose digital I/O pin
89	GPIO_30	IO	1.8	General-purpose digital I/O pin
90	GPIO_34	IO	1.8	General-purpose digital I/O pin
91	GPIO_23	IO	1.8	General-purpose digital I/O pin
92	GPIO_28	IO	1.8	General-purpose digital I/O pin
93	GPIO_27	IO	1.8	General-purpose digital I/O pin
94	GPIO_32	IO	1.8	General-purpose digital I/O pin
95	GPIO_29	IO	1.8	General-purpose digital I/O pin
96	GPIO_26	IO	1.8	General-purpose digital I/O pin
97	GPIO_25	IO	1.8	General-purpose digital I/O pin
98	GPIO_35	IO	1.8	General-purpose digital I/O pin
99	GPIO_24	IO	1.8	General-purpose digital I/O pin
100	GPIO_33	IO	1.8	General-purpose digital I/O pin
101	GPIO_31	IO	1.8	General-purpose digital I/O pin
102	IPQ_MDC	IO	1.8	GPIO pin or MDIO for external switch
103	IPQ_MDIO	IO	1.8	GPIO pin or MDIO for external switch
125	GPIO_39	IO	1.8	General-purpose digital I/O pin
126	GPIO_46	IO	1.8	General-purpose digital I/O pin
128	GPIO_38	IO	1.8	General-purpose digital I/O pin
143	GPIO_19	IO	1.8	General-purpose digital I/O pin
144	GPIO_14	IO	1.8	General-purpose digital I/O pin
145	GPIO_16	IO	1.8	General-purpose digital I/O pin
146	GPIO_17	IO	1.8	General-purpose digital I/O pin
147	GPIO_15	IO	1.8	General-purpose digital I/O pin
148	GPIO_18	IO	1.8	General-purpose digital I/O pin

Pin status on boot

| Pin ID	Pin name	GPIO	Voltage	Internal HW setting	Description
11	SPI0_CLK	GPIO_10	1.8	Pull down 4.7k	Auth enable: 0: no auth 1: auth is required
12	SPI0_MOSI	GPIO_11	1.8	Pull down 4.7k	Fast boot (boot interface select):
9	UART_TXD1	GPIO_21	1.8	Pull down 4.7k	0: SPI-NOR 1: eMMC 2: QSPI(4bit) 3: USB2.0
89	GPIO_30	GPIO_30	1.8	Pull down 4.7k	Watchdog enable: 0: watchdog enabled 1: watchdog disabled (Default)
98	GPIO_35	GPIO_35	1.8	Pull down 100k	Hash in fuse (SW use only): 0: PK hash is stored in boot ROM 1: PK hash is stored in OTP
125	GPIO_39	GPIO_39	1.8	Pull down 100k	Boot ROM boot speed: 0: 24MHz 1: 400MHz
49	IPQ_RST_OUT_N	GPIO_40	1.8	Pull down 100k	Tcxo_mode: 0: xo-mode 1: tcxo-mode
147	GPIO_15	GPIO_15	1.8	Pull down 100k	Use Serial Num: 0: Use OEM ID 1: Use Serial Num
148	GPIO_18	GPIO_18	1.8	Pull up 4.7k	Jtag_boot_en: 0: used as Normal function GPIO 1: used as JTAG
126	GPIO_46	GPIO_46	1.8	Pull down 4.7k	RFA refclk frequency selection: 0: 48MHz 1: 96MHz
20	EMMC_CLK	GPIO_9	1.8	Pull down 4.7k	0: Not force boot from USB 1: force boot from USB

4.2 AI5018H Dimension Mechanical

Unit：mm
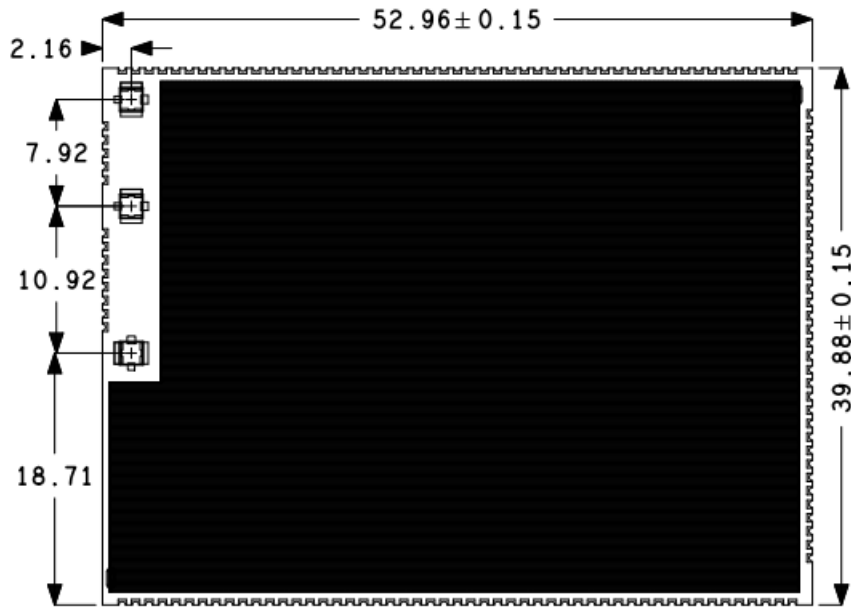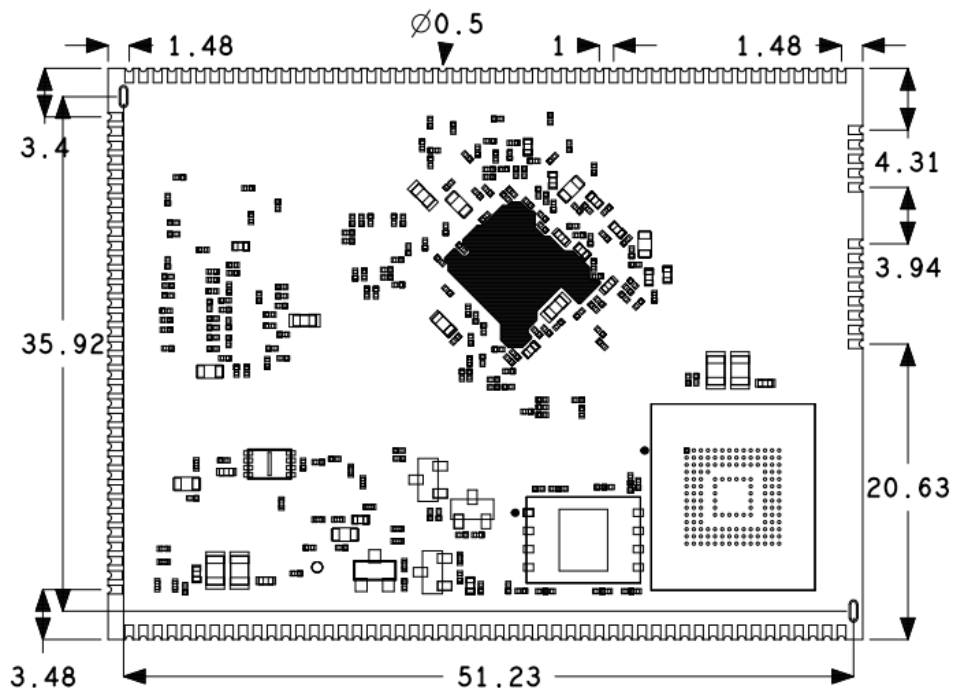

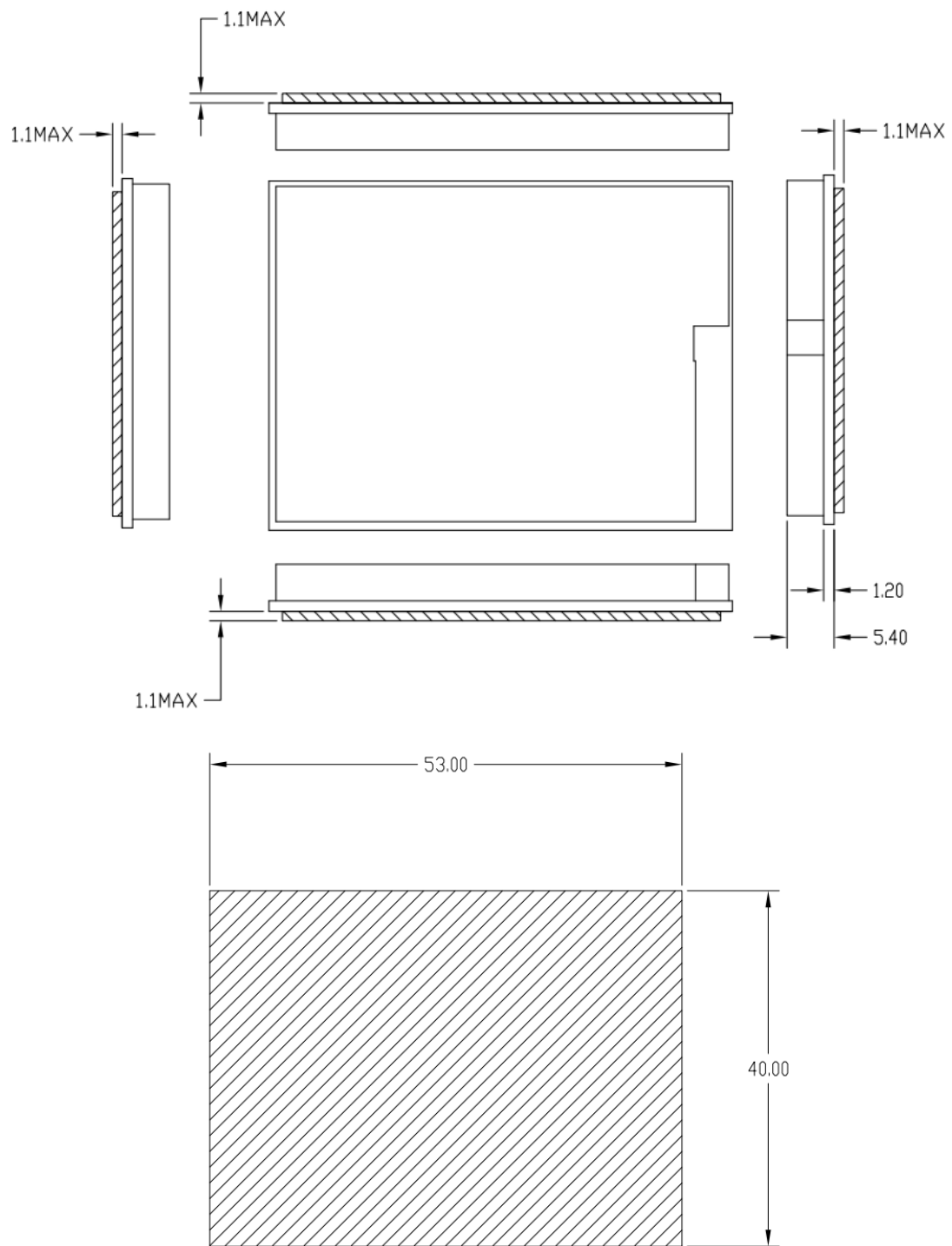**Figure 6. Top view**

Figure 7. Bottom side

Figure 8. Side view

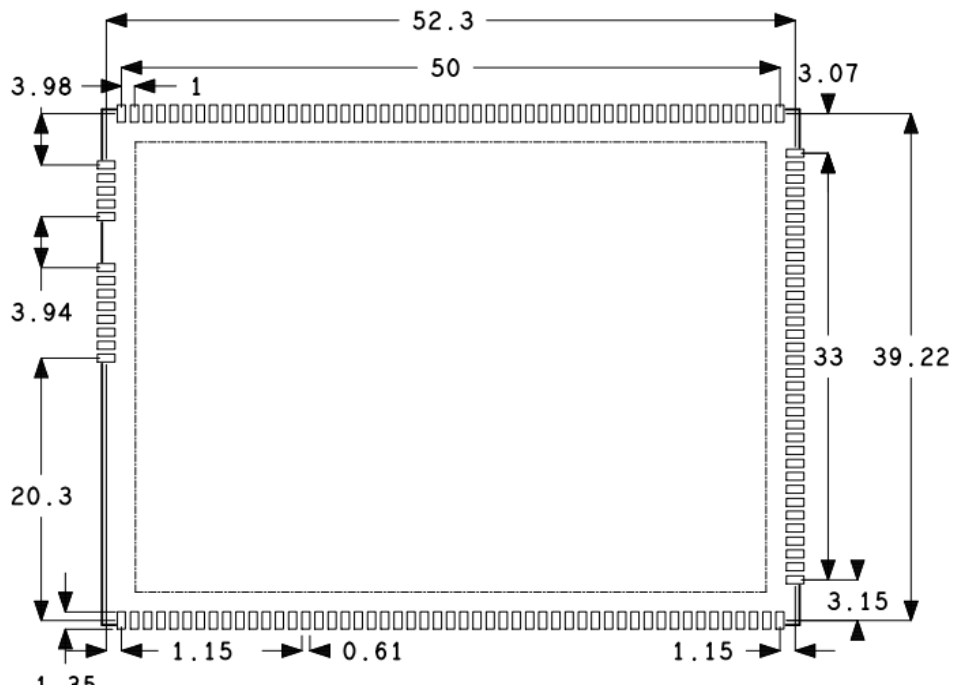# 4.3 Recommended PCB Landing

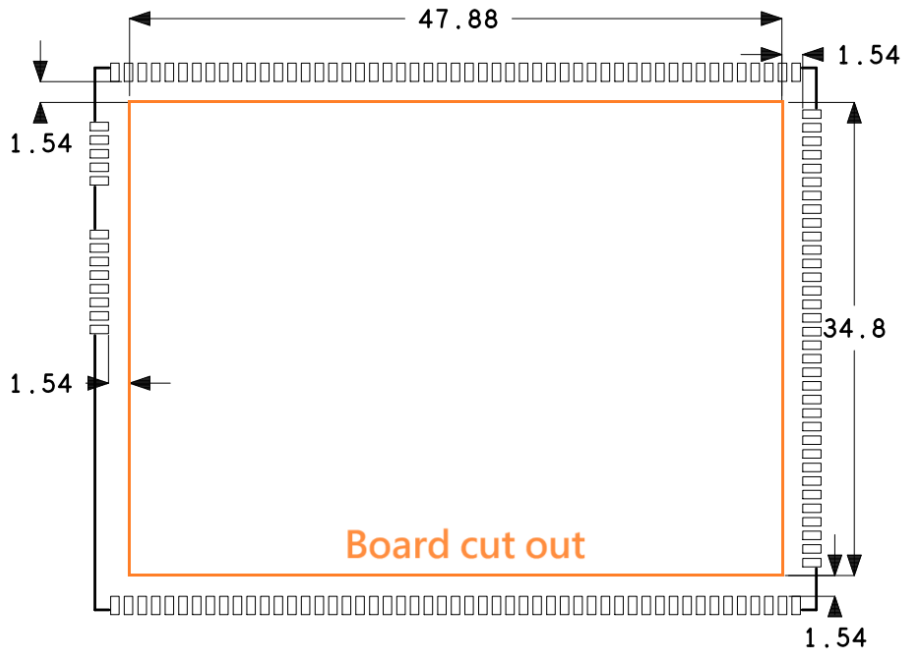
Figure 9. PCB footprint recommend

Figure 10. PCB cutout recommend

5 Regulator

This module is passed on module level to comply with the following standards:

FCC ID：

Item / Region	Service / Standard	Feature
EU/CE	EN 300 328	802.11 b/g/n/ax BT LE / EDR
	EN 62311	MPE
	EN 55032/35	EMC
	EN 301 489-1/-17	RF-EMC
	EN 62368-1	LVD
	CoC letter	
US/FCC	Part 15C	802.11 b/g/n/ax BT LE / EDR
	KDB 44798	MPE
	TCB Certificate	
	US agent	
	Part 15B	

6 Recommended Reflow Profile

Reflow Profile for SiP on board Assembly
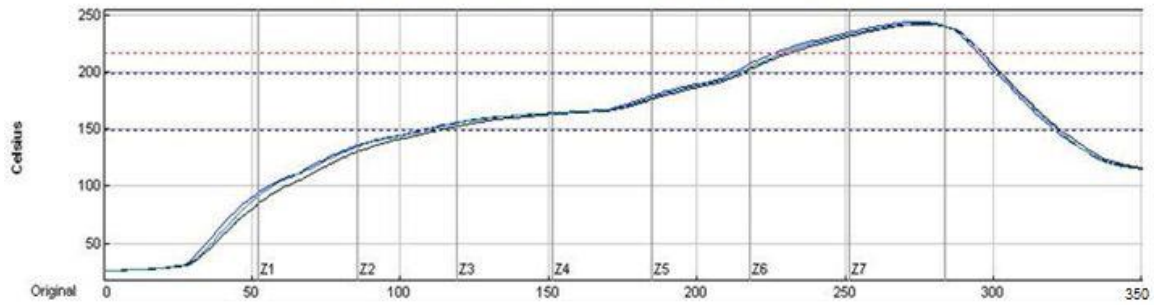
Preheat time	150℃—200℃: 105+/-15sec
Dwell time	Over 220℃: 70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp Up/Down Rate	Up: 3 +0/-2 ℃/ sec Down: 2 +0/-1℃/ sec

7 Module Preparation

7.1   Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

7.2   SMT Preparation

1. Calculated shelf life in sealed bag: 6 months at<40°C and <90% relative humidity (RH).

2. Peak package body temperature: 250°C.

3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.

    A.   Mounted within: 168 hours of factory conditions<30°C /60%RH.

    B.   Stored at≦10%RH with N2 flow box.

4. Devices require baking, before mounting, if:

    A.   Package bag does not keep in vacuumed while first time open.

    B.   Humidity Indicator Card is >10% when read at 23±5°C.

    C.   Expose at 3A condition over 8 hours or expose at 3B condition over 24 hours.

5. If baking is required, devices may be baked for 12 hours at 125±5°C.

8 Package Information

TBD